# SWITCHED CAPACITOR SIGNAL SCALING CIRCUIT

## ABSTRACT OF THE DISCLOSURE

A signal scaling circuit for accurately reducing the effective amplitude of an input signal by a rational factor N/M, where N and M are integers and N < M, is disclosed. An input, reference, bias and output node as well as control circuitry are selectively coupled to M switched capacitor circuits such that N/M scaling may be achieved. Cooperation between the M switched capacitor circuits and the control circuitry divides the M switched capacitors circuits into subsets of N and M — N switched capacitors, respectively. Each subset is then selectively coupled to an input, reference and/or bias signal to produce an output signal having as one of its components an N/M portion of the input signal. Error reduction in the scaled signal is achieved by shuffling the switched capacitor circuits populating each subset after selected time intervals.